IN THE SPECIFICATION

Please replace the paragraph beginning at page 3, line 15 with the following:

The use of operational ~~amplifiers~~ amplifier buffers for amplifiers A1 and A2 described in the Wurcer paper, which is furthermore referenced to a central bias voltage VB, results in bandwidth limitations and additional complexity and power consumption for use as an LNA stage. Also a single-ended signal applied to only one of the two inputs does not produce a balanced differential output signal.

Please replace the paragraph beginning at page 5, line 18 with the following:

An embodiment of a low-noise amplifier as a preamplifier for a variable gain amplifier (VGA) is shown in Figure 4. This particular embodiment is one channel of a dual-channel VGA, so some components may be shared between the channels, the other channel not being shown. The low-noise amplifier (LNA) 10, receives an input signal INH and is biased by a bias generator 12. The LNA may produce differential outputs, a non-inverting output LOP and an inverting output LON. As shown here, these outputs are used [[an]] as inputs to a VGA 14, which produces an amplified signal. A post amplifier 16 may provide selectable gain with an optional output clamp 18 to provide adjustable output voltage limiting.

Please replace the paragraph beginning at page 8, line 3 with the following:

Resistors R2 and R3 are chosen in conjunction with R1 to set the desired LNA gain. Since [[in]] input stage transistors QA and QB are biased at constant current, the voltage impressed on R1 generates signal current that flows through R2 and R3, leading to a proportional voltage drop, or rise, across those devices to the outputs. For a differential input signal, the gain to pins LOP and LON is given by (R2+1/2*R1)/R1 and (R3+1/2*R1)/R1, respectively, for a net gain of (R2+R3+R1)/R1. This gain can also be demonstrated by considering an equivalent differential half-circuit for the amplifier, with the same result.

Please replace the paragraph beginning at page 8, line 19 with the following:

A single-ended input signal applied to the LNA in Figure 5 will not produce a balanced differential output signal if equal values are chosen for R2 and R3. If the input to constant-current biased transistor QB remains at signal ground, then its emitter voltage is

fixed, and the gain to output terminals ~~OPH and OPL~~ LOP and LON are changed. The gain to pin LOP can be shown to be given by the ratio (R2+R1)/R1 and the gain to LON by R3/R1, for this case since the whole input signal is applied to only one side with respect to the signal ground impressed upon the emitter of QB. To achieve balanced outputs, and hence better swing and distortion performance in subsequent stages, values for R2 and R3 are chosen in this design to equate the gains to the two outputs. For the embodiment of Figure 5 with a single-ended input specification, these values are 28 ohms for R2 and 36 ohms for R3 using the R1 value from the example above, for a net gain of 4.5 on each side. This arrangement is in contrast to the prior art shown in figure 3 which only discloses equal values for R56 and R57.

Please replace the paragraph beginning at page 9, line 20 with the following:

The gain A0 is that seen from terminal INH to LON, and is generally one-half the total closed loop gain of the core LNA. The polarity of the gain is inverting, for negative feedback. The actual input impedance realized is this synthesized impedance in parallel with any other biasing resistance and the input impedance of transistor QA in the input stage. Capacitor CFB isolates the DC input levels at input and output and is not absolutely required; [[through]] though it helps with current consumption and load balancing, especially for low valued resistors RFB.

Please replace the paragraph beginning at page 10, line 22 with the following:

As another embodiment involving external components, a ferrite bead may be useful. For example, when a long trace to the input INH is unavoidable, or when the LNA is configured [[a]] as one of two channels and both channels are used to drive external circuits, the ferrite bead FB may provide circuit stability with negligible effect on noise. Other external components may be used with the LNA, these are just set out as examples of the environments in which the LNA may be used.

Please replace the paragraph beginning at page 11, line 8 with the following:

QA and QB are also shown in more detail, being Q15 and Q16 in Figure 6. The input signal INL of Figure [[5]] 6 is the ~~signal~~ ground signal LMD of Figure [[4]] 5. This differential pair-like structure of Q15 and Q16 is a first gain stage. A network of resistors R1, R2 and R3 provide feedback to the emitters of Q15 and Q16 through an electrical

connection between the emitters of Q15 and Q16 and the output node nodes, as described previously.

Please replace the paragraph beginning at page 12, line 1 with the following:

From the base of emitter follower transistor Q8, through Q1, there is a net current gain of β^2 to help supply base current to Q6 for driving peak output currents. This also improves the internal slew-rate for driving the large capacitance associated with Q6. In this design the second stage current bias set by Q4, R40 needs to be large enough to support the peak base-current requirements of transistor Q7. Compensation capacitors C1 and C2 are connected from the high impedance node at Q15 and Q16 collectors to output nodes OPH and OPL, respectively.

Please replace the paragraph beginning at page 12, line 12 with the following:

In the more detailed embodiment shown in Figure 7, a non-linear current mirror is used to bias the second stage amplifier current sources, for further current savings. The output terminal [[OPH]] OPL defines a current through resistor R9, diode connected transistor Q5, and R6. This current is mirrored non-linearly to set the bias current for current-source transistor Q4, which loads the second gain stage. When output OPL rises above its quiescent output level, a larger current is produced in Q5 and an exponentially larger current in Q4. This allows Q4 to supply the needed base current to pull-down transistor Q7, of the output stage, which is simultaneously sinking current to pull output OPH low. The additional current also helps with the transient response, improving the internal slew-rate limit for driving the base of transistor Q7. The net effect is that a lower quiescent current can be established in the second gain stage since more current is available when needed.